





PTO/SB/08A (10-01)  
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Substitute for form 1449A/PTO			<b>Complete if Known</b>	
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (use as many sheets as necessary)			Application / Conf. N .	10/092,051 / 7802
			Filing Date	March 04, 2002
			First Named Inventor	Stephen M. Douglass
			Art Unit	2812
			Examiner Name	Stacy Whitmore
			Attorney Docket Number	X-923 US
Sheet	2	of	7	

OTHER - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), data, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
SW		SAYFE KIAEI et al., "VLSI DESIGN OF DYNAMICALLY RECONFIGURABLE ARRAY PROCESSOR-DRAP," IEEE, February 1989, pp. 2484-2488, V3.6, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
SW		VASON P. SRINI, "FIELD PROGRAMMABLE GATE ARRAY (FPGA) IMPLEMENTATION OF DIGITAL SYSTEMS: AN ALTERNATIVE TO ASIC," IEEE, May 1991, pp. 309-314, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
SW		G. MAKI et al., "A RECONFIGURABLE DATA PATH PROCESSOR," IEEE, August 1991, pp. 18-4.1 to 18-4.4, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
SW		JACOB DAVIDSON, "FPGA IMPLEMENTATION OF RECONFIGURABLE MICROPROCESSOR," IEEE, March 1993, pp. 3.2.1 - 3.2.4, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
SW		CHRISTIAN ISELI et al., "BEYOND SUPERSCALER USING FPGA's," IEEE, April 1993, pp. 486-490, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
SW		P.C. FRENCH et al., "A SELF-RECONFIGURING PROCESSOR," IEEE, July 1993, pp. 50-59, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
SW		Christian Iseli et al., "SPYDER: A RECONFIGURABLE VLIW PROCESSOR USING FPGA's," IEEE, July 1993, pp. 17-24, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
SW		MICHAEL J. WIRTHLIN et al., "THE NANO PROCESSOR: A LOW RESOURCE RECONFIGURABLE PROCESSOR," IEEE, February 1994, pp. 23-30, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
SW		WILLIAM S. CARTER, "THE FUTURE OF PROGRAMMABLE LOGIC and ITS IMPACT ON DIGITAL SYSTEM DESIGN," April 1994, IEEE, pp. 10-16, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
SW		ANDRE DEHON, "DPGA-COUPLED MICROPROCESSORS: COMMODITY ICs FOR THE EARLY 21ST CENTURY," IEEE, February 1994, pp. 31 - 39, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
SW		OSAMA T. ALBAHARNA, "AREA & TIME LIMITATIONS OF FPGA-BASED VIRTUAL HARDWARE," IEEE, April 1994, pp. 184 - 189, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	

Examiner Signature	<i>AG</i> <i>W</i>	Date Considered	3/17/04
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## INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Applicant / Conf. No.	10/092,051 / 7802
Filing Date	March 04, 2002
First Named Inventor	Stephen M. Douglass
Art Unit	2812
Examiner Name	Stacy Whitmore
Attorney Docket Number	X-923 US

### OTHER - NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
SW		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 1994, Revised 1995, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
SW		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 1994, Revised 1995, pp 2-109 to 2-117, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
SW		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 1994, Revised 1995, pp 2-9 to 2-18; 2-187 to 2-199, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
SW		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 1994, Revised 1995, pp 2-107 to 2-108, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
SW		CHRISTIAN ISELI et al., "AC++ COMPILER FOR FPGA CUSTOM EXECUTION UNITS SYNTHESIS," 1995, pp. 173-179, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
SW		INTERNATIONAL BUSINESS MACHINES, "POWERPC 405 EMBEDDED PROCESSOR CORE USER MANUAL," 1996, 5TH Ed., pp. 1-1 TO X-16, International Business Machines, 1580 Rout 52, Bldg. 504, Hopewell Junction, NY 12533-6531.	
SW		YAMIN LI et al., "AIZUP-A PIPELINED PROCESSOR DESIGN & IMPLEMENTATION ON XILINX FPGA CHIP," IEEE, September 1996, pp 98-106, 98-106, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
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SW		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 2000, Ch. 3 pp 3-1 TO 3-117, Xilinx, Inc., 2100 Logic Drive, San Jose, CA 95124	
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SW		XILINX, INC., "VIRTEX II PLATFORM FPGA HANDBOOK, December 6, 2000, v1.1, pp 33-75, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	

Examiner  
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First Named Inventor	Stephen M. Douglass
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**Examiner  
Signature**

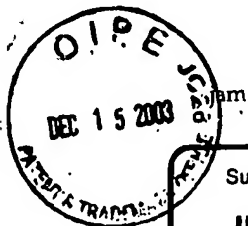
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		Filing Date	March 04, 2002		
		First Named Inventor	Mauna Loa		
		Art Unit	2812		
		Examiner Name	Stacy Whitmore		
Sheet	7	of	7	Attorney Docket Number	X-923 US

U.S. PATENT DOCUMENTS					
Examiner Initials *	Cite No. 1	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code (if known)			
[Handwritten initials]		US- 6,522,167	02-18-03	Ansari et al.	
		US- 6,434,735	08-13-02	Watkins	
		US- 6,588,006	07-01-03	Watkins	
		US- 6,539,508	03-25-03	Patrie et al.	
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		US- 6,611,951	08-26-03	Tetelbaum et al.	
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